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Office Action Dated July 28, 2005

REMARKS

Favorable reconsideration of this application is requested in view of the above amendments and the following remarks. Claim 1 and 6 are hereby amended. Claim 8 is new.

Amendment of claims 1 and 6 are supported, for example, by page 2, lines 2-6. New claim 8 is supported, for example, by the subject matter of claim 1 and page 2, lines 2-6.

Claims 1, 2, 4, 6, and 7 were rejected as being unpatentable over Hulse (US 6,618,847) in view of Miki (US 5,761,076). Applicants traverse this rejection. The combination of Hulse and Miki does not teach a LSI layout method for a LSI design by automatic arrangement wiring of standard cells, including arranging the power supply capacitor cell in a vicinity of the logic gate cell used to determine the capacitance value of the power supply capacitor cell **after** the capacitance value is determined in the providing step, as required by claims 1 and 6.

The Examiner concedes that Hulse fails to teach a capacitance value of the power supply capacitor cell based on the drive load capacity value of an associated logic gate cell.

Miki does not remedy the deficiencies of Hulse. Miki teaches determining a wiring capacitance value in order to determine a delay time used in post layout circuit analysis/test (see column 1, lines 29-32). However, the capacitance calculation is performed with respect to the capacitance of wiring in the LSI which has **already been** arranged by a layout method. Further, the wiring capacitance value taught by Miki cannot be considered equivalent to the capacitance value of the power supply capacitor cell required by claims 1 and 6. The capacitance value calculated by Miki is based on post layout data such as position, wiring length, wiring width, and wiring layers of each of circuit elements (see column 4, lines 46-54). In fact, it would not be possible to calculate the capacitance value taught by Miki before the circuit elements of the LSI are arranged in a layout, as is required by claim 1 and 6. Therefore, neither Miki nor Hulse teach a capacitance value determined before arrangement of the logic gate and power supply capacitor cells.

One knowledgeable in the art would not look to a combination of Hulse and Miki to teach the claimed LSI layout method. The combination would result in a layout method firstly arranging a logic gate cell, secondly determining a power supply capacitor cell, and thirdly arranging the power supply capacitor cell in a space. However, in the resulting method, sufficient space may not be available for arranging the power supply capacitor cell in the vicinity of the logic gate cell which was used to determine the capacitance value, thereby rendering the associated capacitance ineffective in suppressing power supply noise to the associated logic gate cell. For example, Hulse teaches placing a filler cell in a vacant area and later substituting the filler cell with a power supply capacitor cell, so that the power supply capacitor cell can be placed in the vacant area created during layout nearest a power sensitive logic gate area (see Figure 11 and the associated description). The power supply capacitor cells therefore are scattered in a logic gate area. However, since these capacitor cells are arranged in vacant areas, they are not necessarily arranged to correspond to the respective logic gate cell, upon which the capacitance value is based.

Determining the capacitance value prior to arranging cells, as required by claims 1 and 6, effectively suppresses power supply noise to the associated logic gate cell due to the placement of the power supply capacitor cell in the vicinity of the logic gate cell that was used to determine the capacitance value.

Favorable reconsideration of claims 1, 2, 4, 6, and 7 is requested.

Regarding new claim 8, neither Hulse nor Miki teaches that a power supply capacitor cell, having its previously determined capacitance value, is arranged at the time of executing automatic arrangement. Therefore, neither Hulse nor Miki provides a LSI layout method able to dispose a power supply capacitor cell exactly in a vicinity of the logic gate cell used to determine the capacitance value thereof. In fact, Hulse teaches determining the position of the filler cell (that in turn provides a possible location for a power supply capacitor cell) **after** the execution of automatic layout of the logic gate cells. Therefore, Hulse teaches arrangement of the power supply capacitor cells after automatic arrangement. Further, Miki teaches determining a wiring capacitance value **after** automatic arrangement. In fact, Miki uses post layout data to calculate the capacitance value. Therefore, the combination of Hulse and Miki does not enjoy the

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suppression of power supply noise to logic gate cells resulting from the LSI layout method of claim 8.

In view of the above, favorable reconsideration in the form of a notice of allowance is requested. Any questions regarding this communication can be directed to the undersigned attorney, Curtis B. Hamre, Reg. No. 29,165, at (612)455-3802.

Respectfully Submitted,

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Curtis B. Hamre
Reg. No.: 29,165
Hamre, Schumann, Mueller & Larson, P.C.
225 South Sixth Street
Suite 2650
Minneapolis, MN 55402
612.455.3800

DPM:CBH:mfe